

Message Text

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EXCON

E.O. 11652: XGDS-1

TAGS: ESTC, COCOM, BU, JA

SUBJECT: JAPANESE FACOM 230-58 TO BULGARIA - IL 1565

REF: A) OECD PARIS 12270, B) COCOM DOC (76)509

1. THE US AUTHORITIES HAVE REVIEWED THE REFERENCED CASE AND, BASED ON THE PARAMETERS PROVIDED, CONSIDER THE PERFORMANCE OF THE CPU EXCESSIVE FOR THE APPLICATION AND REPRESENTING A SIGNIFICANT RISK FOR DIVERSION. THE PERFORMANCE OF THIS CPU (A PDR OF 98.9 MILLION BITS PER SECOND) EXCEEDS BY A FACTOR OF TWO THE PERFORMANCE OF ANY SINGLE CPU PREVIOUSLY EXPORTED AND EXCEEDS THE COMBINED PDR OF THE LARGEST COMPUTER FACILITY PREVIOUSLY CONSIDERED BY THE COMMITTEE (SERPUKHOV). THE LATTER EXPORT WAS ONLY PERMITTED UNDER THE MOST STRINGENT SAFEGUARD
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CONDITIONS FOR A WORLD RENOWN OPEN HIGH ENERGY PHYSICS

INSTITUTE. HIGH PERFORMANCE CPU'S SUCH AS THE FACOM 230-58 EXCEED KNOWN SOVIET CAPABILITIES (RYAD-1050) BY A FACTOR OF THREE AND ARE NECESSARY FOR MANY TYPES OF SIGNIFICANT MILITARY WEAPONS COMPUTATIONS. ON THIS BASIS, THE US CANNOT AGREE TO THE EXPORT OF THE FACOM 230-58.

2. IF THE JAPANESE DELEGATION WISHES TO RECONSIDER THIS TRANSACTION AND PROPOSE A LOWER PERFORMANCE CPU, THE US WOULD BE PREPARED TO CONSIDER THE CASE ON ITS MERITS. TO SPEED THAT CONSIDERATION IF THE CASE WERE RESUBMITTED, THE US WOULD LIKE CLARIFICATION OF THE FOLLOWING POINTS.

3. FIRST, THE TECHNICAL INFORMATION PROVIDED INDICATES THAT THE F1816A LINE UNIT HAS AN INTERFACE CAPABILITY OF 64 LINES OF 1200 BPS OR A TOTAL OF 76,800 BPS. DOES THIS UNIT OR THE F1820L LIMIT THE NUMBER OF LINES TO SEVEN AS REQUIRED BY NOTE 12(G)(6)(III) OR CAN ADDITIONAL LINES BE CONNECTED WITHOUT THE PROVISION OF ADDITIONAL EQUIPMENT OTHER THAN MODEMS?

4. SECOND, THE TECHNICAL INFORMATION PROVIDED INDICATES THAT THE MD 1200 MODEMS PERMIT FULL DUPLEX OPERATION RESULTING IN AN EFFECTIVE BIT TRANSFER RATE OF 2400 BPS FOR EACH COMMUNICATION CHANNEL OR A TOTAL EFFECTIVE BIT TRANSFER RATE OF 16,800 BPS FOR SEVEN CHANNELS. IS THIS INTERPRETATION CORRECT OR ARE THERE OTHER HARDWARE LIMITATIONS WHICH WOULD NOT PERMIT FULL DUPLEX OPERATION ON EACH COMMUNICATION CHANNEL?

5. THIRD, THE TECHNICAL INFORMATION PROVIDED INDICATES THAT THE EFFECTIVE BIT TRANSFER RATE OF THE F3537 AND F1531N PROGRAMMABLE PROCESSORS IS 4800 BPS. HOWEVER, THE REFERENCED CASE INDICATES A VALUE OF 1200 BPS FOR NOTE 12(G)(5). IS THIS A CORRECT INTERPRETATION OR ARE THERE OTHER EQUIPMENT LIMITATIONS WHICH RESTRICT THE EFFECTIVE BIT TRANSFER RATE OF THE F3537 AND F1531N TO 1200 BPS? ALSO BOTH OF THESE DEVICES APPEAR TO BE DIGITAL COMPUTERS AS DEFINED IN IL 1565 AND REQUIRE THE SUBMISSION OF CERTAIN PERFORMANCE PARAMETERS TO

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THE COMMITTEE.

6. FOURTH, THE EQUIPMENT LIST PROVIDED INDICATES THAT ITEMS 505 THROUGH 519 ARE FOR DEBUGGING THE F1531N AND F3537 TERMINAL PROGRAMS. COULD ADDITIONAL INFORMATION BE PROVIDED ON THIS FUNCTION OR APPLICATION?

7. FIFTH, WHAT IS THE NATURE AND EXTENT OF THE

TECHNICAL TRAINING AND ASSISTANCE THAT IS PROPOSED IN THIS CASE CONCERNING THE OPERATION AND MAINTENANCE OF THE EQUIPMENT, SYSTEM ANALYSIS, DESIGN AND SOFTWARE DEVELOPMENT, AND EQUIPMENT DESIGN AND MANUFACTURING? ALSO, HOW MANY TECHNICANS WILL BE TRAINED AND TO WHAT LEVEL OF COMPETENCE?

8. IN GENERAL, THE US WOULD REQUEST OTHER MEMBER COUNTRIES TO SUBMIT MORE TECHNICAL DATA THE FIRST TIME A NEW COMPUTER SYSTEM WAS SUBMITTED FOR CONSIDERATION IN ORDER TO EXPEDITE THE TECHNICAL ASSESSMENT OF THE CASE. FOR THE REFERENCED CASE US TECHNICANS WERE NOT ABLE TO ASSESS THE CPU BUS RATE AND PDR BECAUSE INFORMATION ON THE NUMBER OF BITS IN A FIXED OR FLOATING POINT INSTRUCTION AND THE MEMORY TO REGISTER INSTRUCTION EXECUTION TIMES (FLOATING POINT ADD) WERE NOT PROVIDED. ALSO THERE WERE NO TECHNICAL DETAILS PROVIDED ON THE OPERATING AND PERFORMANCE CHARACTERISTICS OF ANY CACHE MEMORY, OVERLAPPING OF INSTRUCTION FETCHING AND EXECUTION, AND MEMORY INTERLEAVING. THE US POSITION INDICATED IN PARA 1 ABOVE WAS BASED ON THE INFORMATION SUPPLIED BY THE JAPANESE DELEGATION BUT NOT INDEPENDENTLY VERIFIED.

9. FYI: THE US IS NOT PREPARED UNDER ANY CIRCUMSTANCES TO APPROVE A CASE FOR SUCH A HIGH PERFORMANCE CPU. CERTAINLY THERE IS NO JUSTIFICATION IN THE SUPPLIED DOCUMENTS AS TO WHY SUCH A LARGE CPU IS REQUIRED. HOWEVER, THE DEL CAN PRIVATELY ASSURE THE JAPANESE DEL THAT A SMALLER SYSTEM BASED ON THE FACOM 230-48 (PDR ABOUT 15) WOULD BE CONSIDERED OR POSSIBLY A SYSTEM BASED ON A CPU OF UP TO A PDR OF 32 WITH THE PROPOSED SAFEGUARDS. IF JAPANESE DECIDE TO RESUBMIT CASE WITH

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SMALLER CPU, PLEASE INDICATE TO THEM THAT INFORMATION REQUESTED IN PARAS 3 TO 8 IS NECESSARY FOR FASTER US REVIEW. DO NOT TELL THE JAPANESE, BUT FOR A SYSTEM WITH A PDR GREATER THAN 32, RESIDENCY AND OTHER SAFEGUARDS WOULD PROBABLY BE REQUIRED WITH NO ASSURANCE OF FAVORABLE CONSIDERATION BY US. CURRENTLY, US HAS UNDER CONSIDERATION A 370/158 CASE (PDR ABOUT 43) WITH COMPARABLE PERIPHERALS BUT NO DECISION HAS YET BEEN REACHED. IF THIS CASE IS APPROVED IT WILL REQUIRE RESIDENCY AND OTHER SAFEGUARDS COMPARABLE TO KAMA RIVER AND AEROFLOT. MAW

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